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1. Your reference	P2844
2. Patent application number *(The Patent Office will fill in this part)*	14 JUN 1999 — 9913713.5
3. Full name, address and postcode of the or of each applicant *(underline all surnames)*	The Secretary of State for Defence Defence Evaluation & Research Agency Ively Road Farnborough, Hampshire GU14 0LX
Patents ADP number *(if you know it)*	~~2576002~~ 7349996001 Rdes
If the applicant is a corporate body, give the country/state of its incorporation	United Kingdom
4. Title of the invention	Method of Fabricating a Semiconductor Device
5. Name of your agent *(if you have one)*	A. O. Bowdery et al
"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*	Intellectual Property Department Building X 92 DERA Farnborough Ively Road Farnborough Hampshire GU14 0LX
Patents ADP number *(if you know it)*	~~2576002~~ 7679590001 Rdes

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11.

I request the grant of a patent on the basis of this application.

Signature A. W. S. Williams Date 14/06/99

12. Name and daytime telephone number of person to contact in the United Kingdom: A. O. Bowdery 01252 392398

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METHOD OF FABRICATING A SEMICONDUCTOR DEVICE

The invention relates to a method of fabricating a semiconductor device having at least one epitaxial layer which is tapered, or equivalently flared, in a plane perpendicular to the plane of the layer on which it is grown. More particularly, although not exclusively, it may be used to fabricate a semiconductor optical slab-waveguide having a core layer which is tapered in a plane perpendicular to the plane of the layer on it is grown.

Opto-electronic systems contain optical fibres and opto-electronic semiconductor devices such as lasers, amplifiers, modulators, detectors and switches. The size and shape of the optical modes supported by optical fibres are significantly different to those within opto-electronic semiconductor devices, and this results in modal mismatch and high optical losses when optical radiation is coupled between such devices and fibres.

One technology which reduces such optical losses involves the use of a microlens placed between the opto-electronic semiconductor device and the optical fibre. The microlens changes the size of the optical mode output by the opto-electronic semiconductor device or optical fibre, but not the shape of the mode. Another technology involves the use of an optical mode-converting waveguide placed between the opto-electronic semiconductor device and the optical fibre. Both of these technologies demand very high alignment tolerances with the result that the alignment of the components can represent the most significant part of the total cost of an opto-electronic system.

A third technology which reduces coupling losses involves the use of opto-electronic semiconductor devices having output waveguides with a two-dimensional tapered thickness profile between the active part of the device and the output facet. This tapering of the output waveguide allows the relatively small (0.5 to 2.0 μm) and sometimos highly asymmetric optical mode from the active part of an opto-electronic semiconductor device to be closely matched to the larger (6 to 10 μm), circularly symmetric optical mode supported by an optical fibre.

Lateral tapering of the output waveguide of an opto-electronic semiconductor device, i.e. tapering in a plane parallel to a substrate surface, may be achieved using known

semiconductor processing techniques such as photolithography and chemical etching. This is carried out after epitaxial growth of the wafer from which the device is made. Tapering the core layer of a waveguide in a plane perpendicular to the plane of epitaxial layer on which it is grown is more difficult and involves controlling the thickness of the core layer during wafer growth.

Methods currently used for producing vertically tapered and flared semiconductor optical waveguides are described by Moerman in IEEE Journal of Selected Topics in Quantum Electronics, Volume 3 , Number 6, pp 1308 - 1320 and may be classified under three main headings, as follows:

1. Etching and re-growth techniques.

In these techniques, epitaxial growth of the wafer is stopped after deposition of the core layer of the waveguide. The wafer is then removed from the wafer growth apparatus and the core layer is etched to produce the required taper profile. The wafer is then replaced in the growth apparatus and the upper guiding layer is grown over the etched core layer. These techniques have the following disadvantages. First, the overall processing is complex and time-consuming. Second, removal of the partially-grown wafer from the growth apparatus and etching the waveguide core layer introduces contamination into the waveguide, increasing optical losses and reducing yield. Third, these methods have very low reproducibility. In one such method, known as dip-etching, it not possible to process the whole surface of a wafer.

2. Impurity-induced disordering.

This is a technique for producing vertically tapered waveguides starting with a waveguide in which the core layer has a uniform thickness. This technique is limited in that the initial uniform waveguide must have a core layer consisting of a multiple quantum-well region. Zinc is diffused into the waveguide through the upper guiding layer and penetrates the core layer to depth which varies with lateral position, i.e. position in the plane of the epitaxial layers. Where zinc has diffused, the refractive index of the core layer is reduced to that of the guiding layers, producing vertical tapering of the waveguide. This technique has low reproducibility, and the resulting waveguides have significant optical loss in the regions where zinc diffusion occurs. It is also limited in respect of the material systems that may be used.

3. Epitaxial techniques.

Several techniques exist in which the tapered core layer and upper guiding layer of a waveguide may be grown in a single step. For example, a temperature gradient introduced in the plane of a wafer consisting of a substrate and a lower guiding layer during the growth of the core layer by molecular beam epitaxy (MBE) may be used to control the thickness of that layer. In this technique it is very difficult to control the compositional uniformity of ternary and quaternary compounds across the temperature gradient and materials having a low melting point or requiring a high growth temperature may have a narrow range of suitable growth temperatures. This places limits on the temperature gradients that may be employed.

Another epitaxial technique is known as "growth-on-a-ridge". By standard etching methods a ridge of varying width may be produced on a wafer comprising a substrate and a lower guiding layer. Due to surface diffusion properties of metal-organic vapour-phase epitaxy (MOVPE), the growth rate of the remaining waveguide layers increases as the width of the ridge decreases, producing a tapered waveguide. This technique involves complicated and time-consuming wafer processing before epitaxial growth of the core and upper guiding layers can take place.

Yet another epitaxial technique is shadow-mask MOVPE growth using a dielectric mask. In this technique, a patterned dielectric mask is deposited onto a wafer. During MOVPE epitaxial growth, deposition takes place through a window in the shadow mask. The lateral thickness of the layer deposited underneath the shadow mask may be controlled by varying the lateral dimensions of the window, the distance between the mask and the substrate, and the reactor pressure. This technique involves an additional growth step of growing the dielectric mask and an additional processing step to remove it. Although a mechanical shadow mask may be used instead of a dielectric mask, MOVPE growth inevitably results in compositional non-uniformity within the tapered layer due to the unequal diffusion lengths of the reaction gases in MOVPE growth. This results in refractive index non-uniformity within the tapered layer which adversely affects the guiding of light within that layer. Also, exposure of the wafer to the atmosphere during mask insertion and removal may result in contamination of the wafer. A further disadvantage is that deposition of material on the mask itself necessitates mask cleaning or replacement.

It is an object of the invention to provide an alternative process for fabricating a semiconductor optical slab-waveguide in which the core layer of the waveguide is tapered in a plane normal to the plane of the substrate upon which the epitaxial layers comprising the waveguide are deposited.

Another object of the invention is to provide an alternative process for fabricating a semiconductor device having at least one epitaxial layer which is tapered in a plane normal to the plane of the substrate on which the device is grown.

The invention provides a method of fabricating a semiconductor device.

The invention provides several advantages. First, the process allows the fabrication of a passive ridge waveguide incorporating a core layer which is tapered in two dimensions by means of a single epitaxial growth step starting from a standard substrate followed by standard wafer processing. As there are no interruptions to the epitaxial growth step and no post-processing steps are required to obtain vertical tapering of the core layer, the process is relatively simple and rapid allowing relatively inexpensive production on an industrial scale. The single-step epitaxial growth facilitated by the invention also eliminates contamination associated with interruption of epitaxial growth, improving yield. Second, compositional inhomogeneities in the tapered region of the waveguide, which occur in shadow mask growth by MOVPE, are avoided due to the absence of gas phase reactions. This is because epitaxial growth is carried out by chemical beam epitaxy (CBE), thus avoiding uncontrolled changes in thickness and refractive index that may affect the guiding properties ofa waveguide or increase its optical loss. Third, the process allows the fabrication of tapered waveguide core layers which taper down continuously from the thick part of the core to the thin part. In tapered waveguides grown using a shadow mask and MOVPE, the core layer thickness first increases before tapering to the thin part of the core. This effect adversely affects the guiding properties and loss of the waveguide and is avoided in the present process. Fourth, there is no polycrystalline growth on the shadow mask used during the epitaxial growth stage of the process. This allows a shadow mask to be re-used because mask definition is maintained both during and after epitaxial growth. This is in contrast to epitaxial growth by molecular beam epitaxy (MBE) where significant polycrystalline growth occurs on the shadow mask causing unwanted shadowing effects.

When the process is employed to fabricate waveguides of aluminium gallium arsenide (AlGaAs) and gallium arsenide (GaAs) it preferably uses triethyl gallium (TEGa) or tri-isopropyl gallium (TIPGa) as the gallium source, the ethyl dimethylamine adduct of alane (EDMAAl) as the aluminium source and thermally-cracked arsine as the arsenic source. In order to reduce impurities in the growth crystal and so improve optical characteristics of the resulting device, the growth is preferably conducted at a temperature in the range 500 to 600 °C.

In the case of waveguides based on indium phosphide (InP) and indium gallium arsenide phosphide (InGaAsP) the process preferably uses trimethyl indium (TMIn), trimethyl gallium (TMGa), arsine and phosphine as the sources of indium, gallium, arsenic and phosphorus respectively.

In order that the invention may be more fully understood, embodiments thereof will now be described, by way of example only, with reference to the accompanying drawings in which:

Figures 1 to 4 show the principal stages in a process according to the invention for producing a semiconductor optical waveguide with a core layer which is tapered in two dimensions,

Figure 5 shows a vertical section of a mechanical apparatus used during production of the waveguide,

Figure 6 shows a vertical section of a shadow mask used in the process,

Figure 7 shows a plan view of the shadow mask, and

Figure 8 shows the structure of an opto-electronic semiconductor modulator which may also be produced by a process of the invention and which has a core layer which is tapered in two dimensions.

Referring to Figure 1, there is shown a portion of a vertical section through a gallium arsenide (GaAs) substrate wafer 10. The substrate 10 is prepared for epitaxial growth

according to standard procedures familiar to those skilled in the art of semiconductor device fabrication. The substrate 10 is mounted in a molybdenum holder (not shown). The mounted substrate 10 is loaded into a chemical beam epitaxy (CBE) apparatus (not shown) and is then stored under ultra-high vacuum (UHV). It is then loaded into the growth chamber of the CBE apparatus under UHV conditions and heated to approximately 650 °C under an arsenic overpressure to remove oxide deposits on the surface whilst maintaining a stable surface and avoiding roughening. The temperature of the substrate 10 is then set to a growth temperature of approximately 540 °C to reduce unintentional incorporation of impurities during CBE growth using the preferred sources. Referring to Figure 2, the following layers are successively deposited by CBE uniformly over the surface of the substrate 10 in the following order:

a 0.5 μm layer 11 of GaAs,
a 3.5 μm layer 12 of AlGaAs having an aluminium mole fraction of 0.05 ± 0.005,
a 0.4 μm layer 13 of AlGaAs having an aluminium mole fraction of 0.3 ± 0.03, and
a 1.8 μm layer 14 of GaAs.

During CBE growth of the layers 11 to 14, the CBE reactor pressure is kept below 10^{-3} Torr so that gas phase reactions are avoided and the substrate 10 is rotated at 60 revolutions per minute. The layer 11 is a buffer layer which separates waveguide layers from the substrate 10. Layers 12 and 13 form lower guiding layers in the finished waveguide. The thickness of layer 14 is equal to that of a thin region of the tapered core layer in the finished waveguide. The substrate 10 and the layers 11 to 14 constitute a partially grown wafer 28. Following deposition of the layer 14 the arsine flux is switched off and the temperature of the wafer 28 is reduced to 200 °C to avoid roughening of its upper surface.

Referring now to Figure 3, a silicon dioxide coated silicon shadow mask 22 (of which an end portion is shown) having a series of apertures such as 23 is mounted in intimate contact with a tantalum spacer 20 in a molydenum carrier (not shown). The shadow mask 22 and spacer 20 are loaded into the growth chamber of the CBE apparatus under UHV conditions and clamped into position. The spacer 20 separates the shadow mask 22 from the exposed surface of the layer 14 by a distance of 100 μm. The arsine flux is switched on and the temperature of the wafer 28 is returned toa

growth temperature which is the original growth temperature (540 °C) corrected for an increase in surface temperature of the wafer 28 as a result of the shadow mask 22 reducing heat loss from it. CBE growth is then resumed. The environmental conditions in the CBE apparatus are such that CBE growth will take place on a chemically appropriate surface (i.e. layer 14) but not on an inappropriate surface (i.e. the surface of the mask 22). A 4 μm layer 16 of GaAs is grown over the layer 14 through the apertures in the shadow mask 22. In regions such as 29, close to the edges of the apertures in the mask 22, the growth rate is reduced so that the finished layer 16 has a thickness profile in the region 29 which tapers smoothly from zero to 4 μm over a lateral distance of approximately 1000 μm. Layers 14 and 16 form a homogeneous core layer 18 having tapered regions such as 15. It is believed that the profile of the tapers such as 15 is dominated by the angle at which chemical beams arrive at the wafer 28 during epitaxial growth. The length of the tapers 15 may be controlled by changing the thickness of the spacer 20 and the angle at which the chemical beams arrive at the wafer 28. This is in contrast to shadow mask growth by MOVPE where the taper profile is dominated by the geometry of apertures in the shadow mask and gas phase reactions so that the tapers' lengths may be limited by the diffusion length of molecules on the surface at a given temperature.

Growth of layer 16 is terminated by switching off the flux of group III-containing species to the growth chamber of the CBE apparatus. The temperature of the wafer 30 is reduced to 200 °C and the arsine supply to the CBE apparatus is switched off. The spacer 20 and shadow mask 22 are removed under UHV conditions. The arsine flux is then switched on and the temperature of the wafer 30 is returned to approximately 540 °C. CBE growth is then resumed. Referring now to Figure 4, a 1.2 μm thick layer 24 of AlGaAs having an aluminium mole fraction of 0.2 ± 0.02 is deposited on the upper surface of the layer 18 forming an upper guiding layer. A 0.1 μm capping layer 26 of GaAs is deposited uniformly over the upper guiding layer 24. Epitaxial growth is then complete and the finished wafer 31 is removed from the CBE apparatus.

Lateral tapering of the waveguide, i.e. tapering in a plane parallel to the plane of the surface of the substrate 10, is then carried out by photolithography and reactive-ion etching in order to produce a laterally tapered ridge waveguide. Accurate photolithography may be achieved using a minimal length tapered alignment feature

deposited through the shadow mask 22. The completed device is a passive ridge waveguide incorporating a core region which is tapered in two dimensions and which converts the size of an optical mode guided within it.

The CBE apparatus includes a stainless steel growth chamber having a rotatable heated substrate assembly, a gas inlet manifold, a stainless steel storage chamber for storage of substrates and shadow masks, a stainless steel loadlock chamber for loading and unloading substrates and shadow masks and a transfer mechanism for transferring substrates and shadow masks between chambers. The CBE apparatus also includes vacuum pumps to maintain UHV conditions within the chambers of the apparatus. During epitaxial growth, group III and group V chemical beams impinge on the surface of the substrate 10 at 45°.

Referring to Figure 5, there is shown a vertical section of a mechanical apparatus 50 which is used to hold the substrate 10, the spacer 20 and the shadow mask 22 within the CBE apparatus during epitaxial growth. The substrate 10 is mounted on a molybdenum carrier 52 and is secured in position by two tantalum springs 54. The substrate 10 has a major flat which sits firmly against a flat surface 56 of the carrier 52. The carrier 52 is attached to a heater assembly 58 by three pins such as 60. The spacer 20 and shadow mask 22 are mounted in a molybdenum holder 62 which is mounted onto the apparatus 50 over the substrate 10 by three pins such as 64, the spacer 20 being in contact with the substrate 10 around its edge. A clamping ring 66 having three springs 68 is mounted over the shadow mask 20 on the three pins to ensure contact between the spacer 20 and the substrate 10. The apparatus 50 gives minimum rotational error and accurate registration between the substrate 10 and shadow mask 22.

Referring now to Figure 6, there is shown a vertical section of the shadow mask 22. The mask 22 is fabricated from a silicon wafer having a thickness of 450 μm and a diameter of 75 mm. By standard procedures of photolithography and chemical etching, the <111> planes of the silicon wafer are etched to produce a series of apertures such as 23 with sloping sides such as 90 which are inclined at 54.7° to the plane of the silicon wafer. The remaining silicon 92 is coated with a thermal oxide film 91. Due to the chemical nature of CBE growth, there is no polycrystalline growth on the shadow mask 22 during epitaxial growth of layer 16. This is because

decomposition of metal-containing alkyls does not occur on the oxide surface 91 of the mask 22 over a large temperature range in CBE growth. Figure 7 shows a plan view of the shadow mask 22 and also indicates the apertures 23 and the position of the substrate 10. The shadow mask 22 includes apertures 40 for the intrusion of the springs 54 and flat surface 56. The mask 22 also has holes 41 to enable it to be attached to the molybdenum carrier 62.

In a further embodiment of the invention, the process may be used to fabricate a tapered waveguide in which the guiding layers are of indium gallium arsenide phosphide (InGaAsP) and the tapered core layer is of indium phosphide (InP). Such a waveguide may be used for guiding and reshaping optical modes with wavelengths around 1.3 or 1.5 μm. In yet further embodiments of the invention, the process may be used to fabricate vertically tapered waveguides having core layers of indium arsenide (InAs), gallium antimonide (GaSb) or indium antimonide (InSb) for use with radiation having wavelengths between 1 and 8 μm.

The process of the invention may also be used to fabricate other semiconductor devices incorporating at least one tapered layer in a single epitaxial growth step. Figure 8 shows the structure of an opto-electronic semiconductor modulator 100 which may be fabricated by the process. The modulator 100 is fabricated as follows. An n-type GaAs substrate wafer 110 is prepared, mounted and loaded into a CBE apparatus as described above. The following epitaxial layers are then successively deposited on the wafer 110 by CBE in the following order:

a 0.5 μm layer 112 of n-type GaAs having a doping density of 10^{18} cm^{-3},
a 3.5 μm layer 114 of n-type AlGaAs having an aluminium mole fraction of 0.05 ± 0.005 and a doping density of 10^{18} cm^{-3},
a 0.3 μm layer 116 of n-type AlGaAs having an aluminium mole fraction of 0.3 ± 0.03 and a doping density of 10^{18} cm^{-3},
a 0.1 μm layer 118 of n-type AlGaAs having an aluminium mole fraction of 0.3 ± 0.03 and a doping density of 10^{17} cm^{-3},
a layer 120 of undoped GaAs having a tapered region 126 in which the thickness of the layer 120 increases from 1.8 μm to 5.8 μm over a lateral distance of approximately 1000 μm and which is formed using a spacer and shadow mask as described above,

a 1.2 μm layer 122 of undoped AlGaAs having an aluminium mole fraction of 0.2 ± 0.02, and

a 0.1 μm capping layer 124 of undoped GaAs.

CLAIMS

1. A method of fabricating a semiconductor device.

2. A semiconductor device.

FIG. 1.

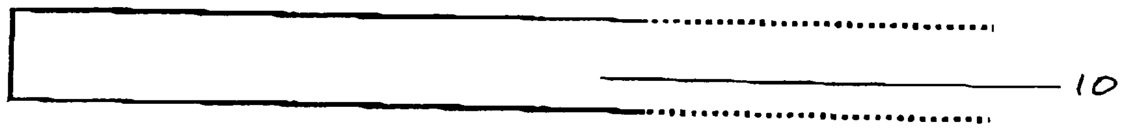

FIG 2

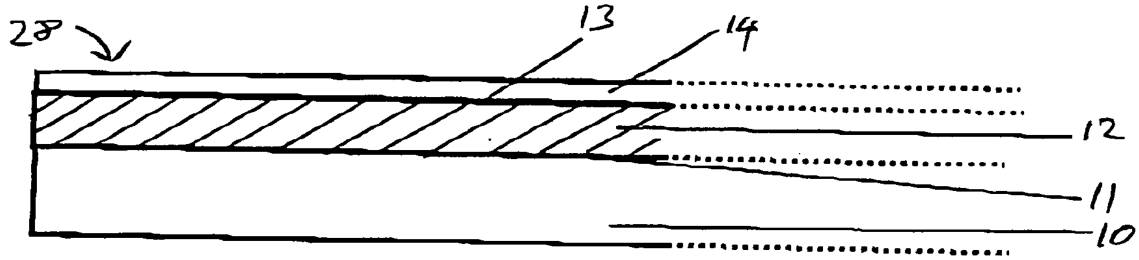

FIG. 3

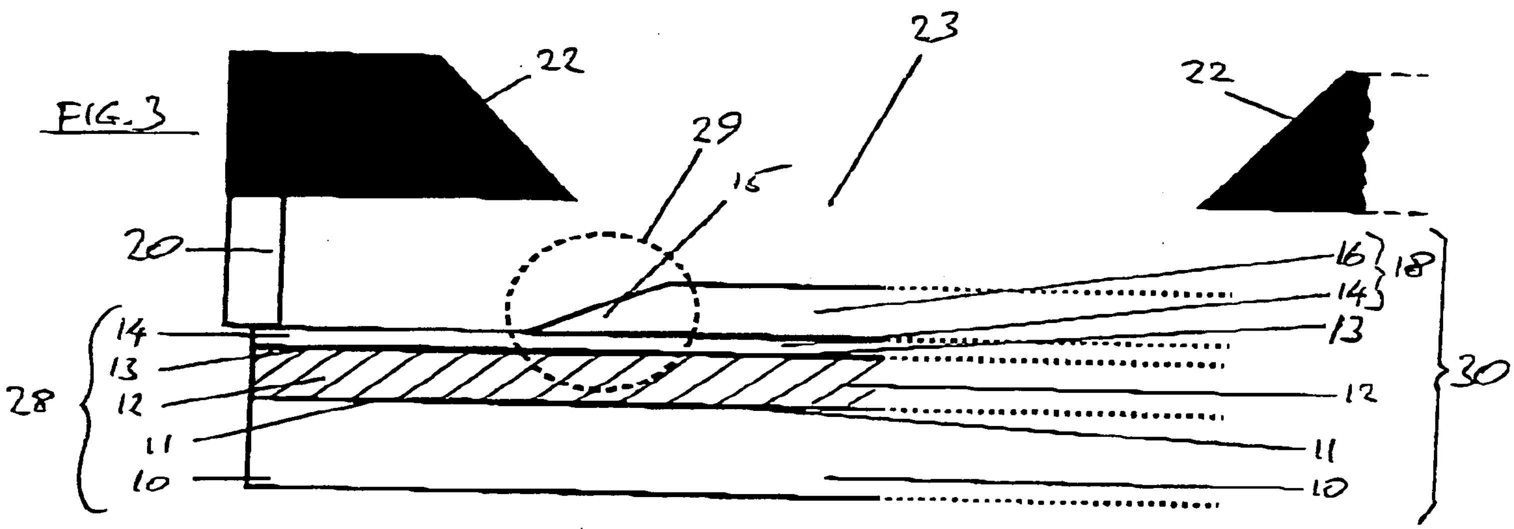

FIG. 4

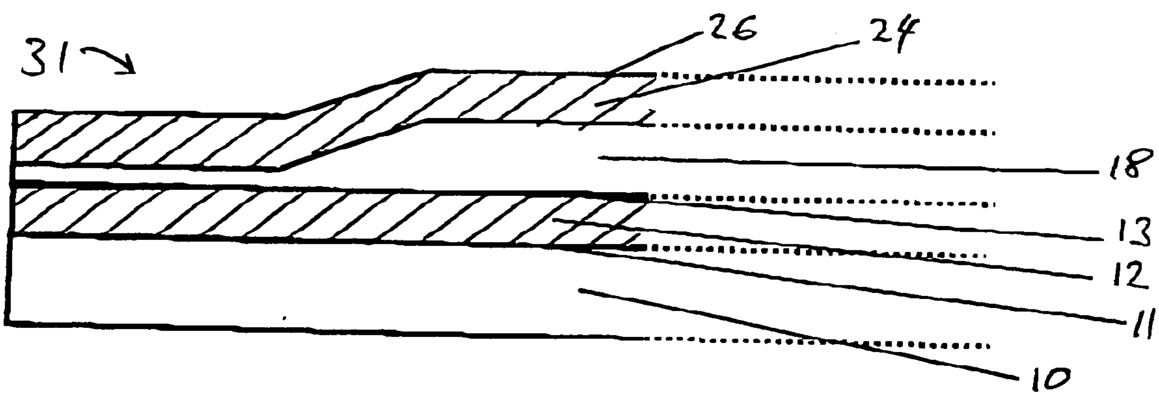

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FIG. 5

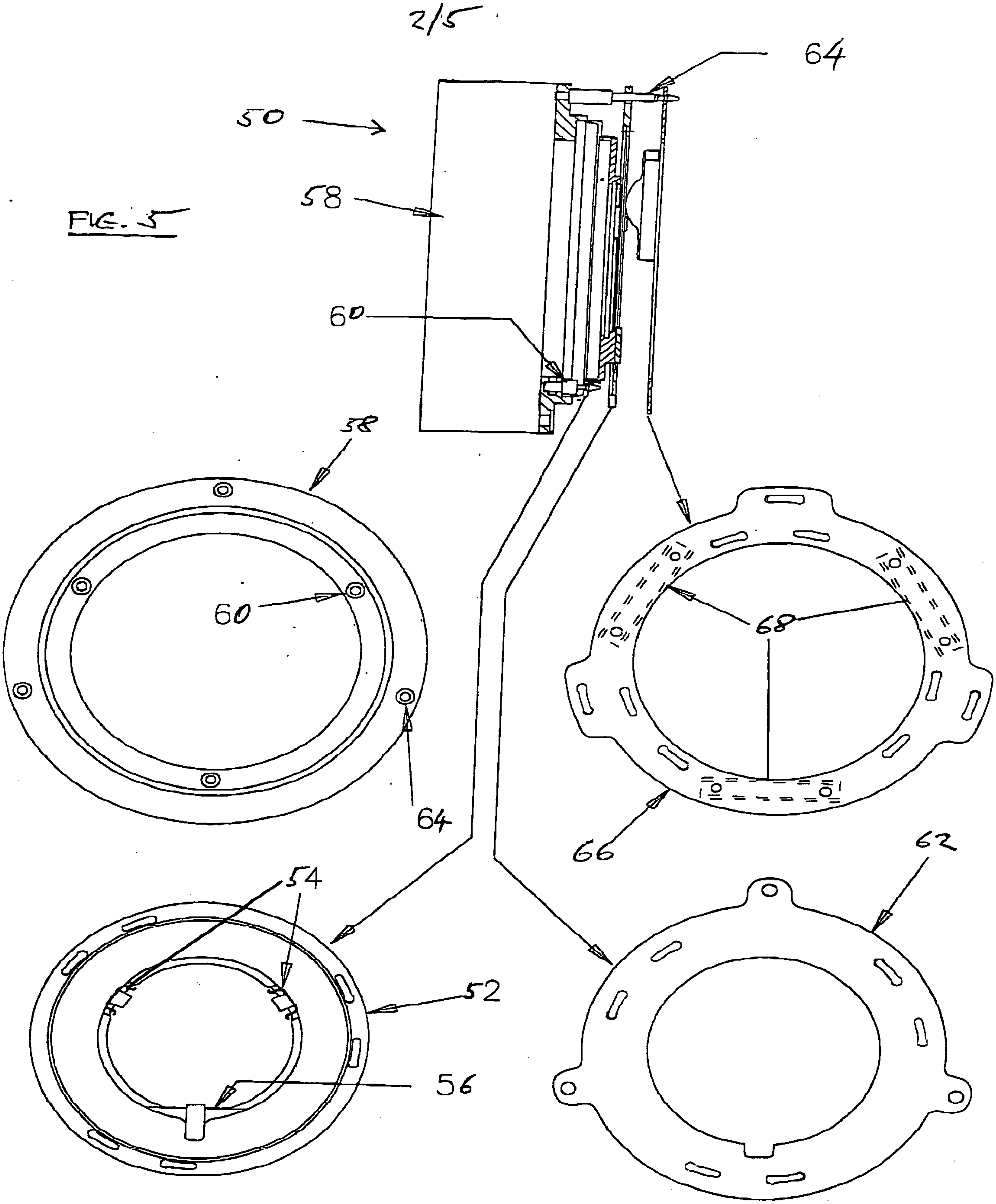

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FIG. 6

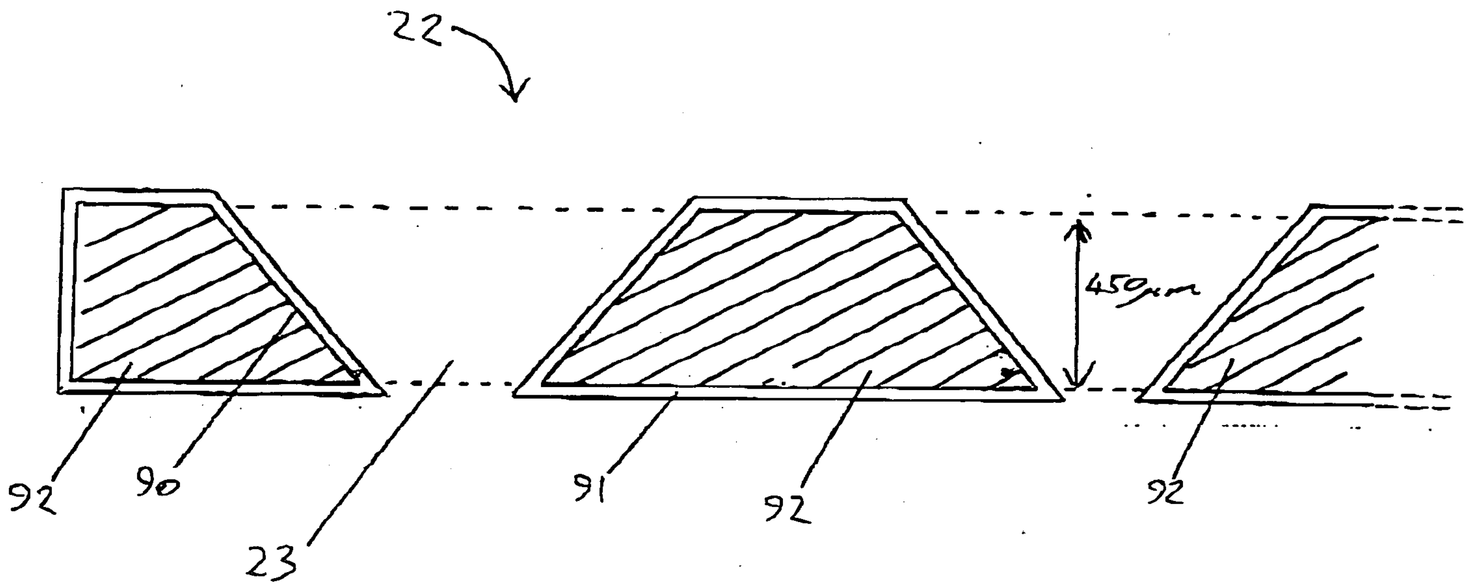


FIG. 7

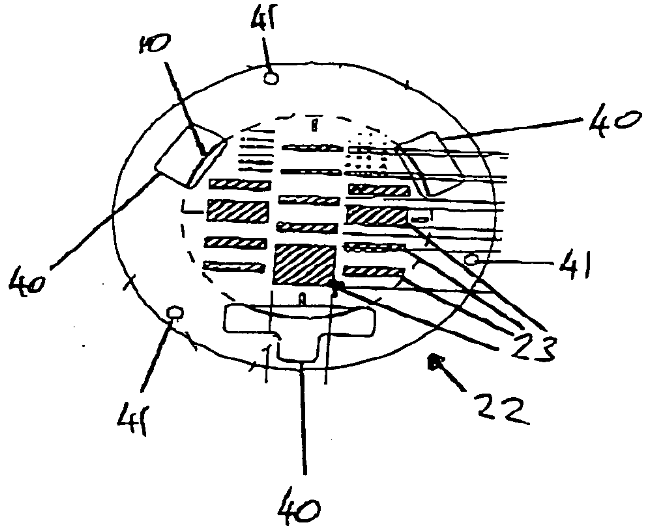
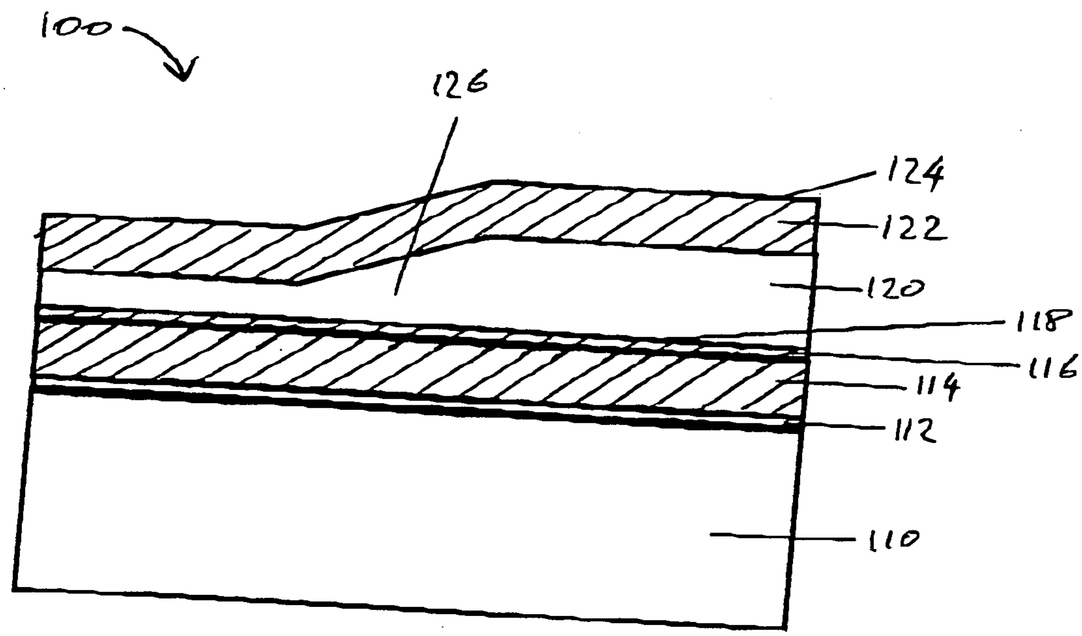


FIG. 8



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